

REVIEW

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Heterogeneous integration by adhesive bonding

Masayoshi Esashi^{1*} and Shuji Tanaka²

Abstract

Wafer level adhesive bonding has been applied for the fabrication of micro systems which have heterogeneous components on LSI. Films or MEMS devices formed on a carrier wafer are transferred on a LSI wafer, which makes versatile heterogeneous integration possible. Film transfer processes and device transfer processes have been developed and applied to mirror array, resonator, piezoelectric switch, IR imager, tactile sensor, electron source and so on. Selective bonding to transfer devices on one carrier wafer to multiple LSI wafers has been developed.

Keywords: Integrated MEMS; Heterogeneous integration; Adhesive bonding; Wafer level transfer

Introduction

Integrated MEMS (micro electro mechanical systems) as capacitive sensors and arrayed display have been produced successfully. MEMS as switches and filters fabricated on CMOS LSI are needed for future multi-band wireless systems, in which good mechanical properties or piezoelectric materials are required for the MEMS and state of the art for the LSI. Such heterogeneous integration can be performed by transferring MEMS devices or a film fabricated on a carrier wafer to a LSI wafer by adhesive bonding as shown in Figure 1. The LSI wafer is not damaged during the MEMS fabrication because the MEMS and the film are fabricated on a separated carrier wafer and the adhesive bonding can be carried out at low temperature. MEMS on LSI is encapsulated by WLP (wafer level packaging) [1] and finally diced to each chips.

The wafer level transfer process can be low cost comparing chip level processes, however for different chip size of MEMS from that of LSI selective transfer process described in V is needed for cost-effective manufacturing.

The wafer level integration by the adhesive bonding was used in the past. Figure 2 is an example of this technology presented in 1984 [2]. Stacked CMOS LSI was fabricated by bonding a PMOS wafer to a NMOS wafer with polyimide.

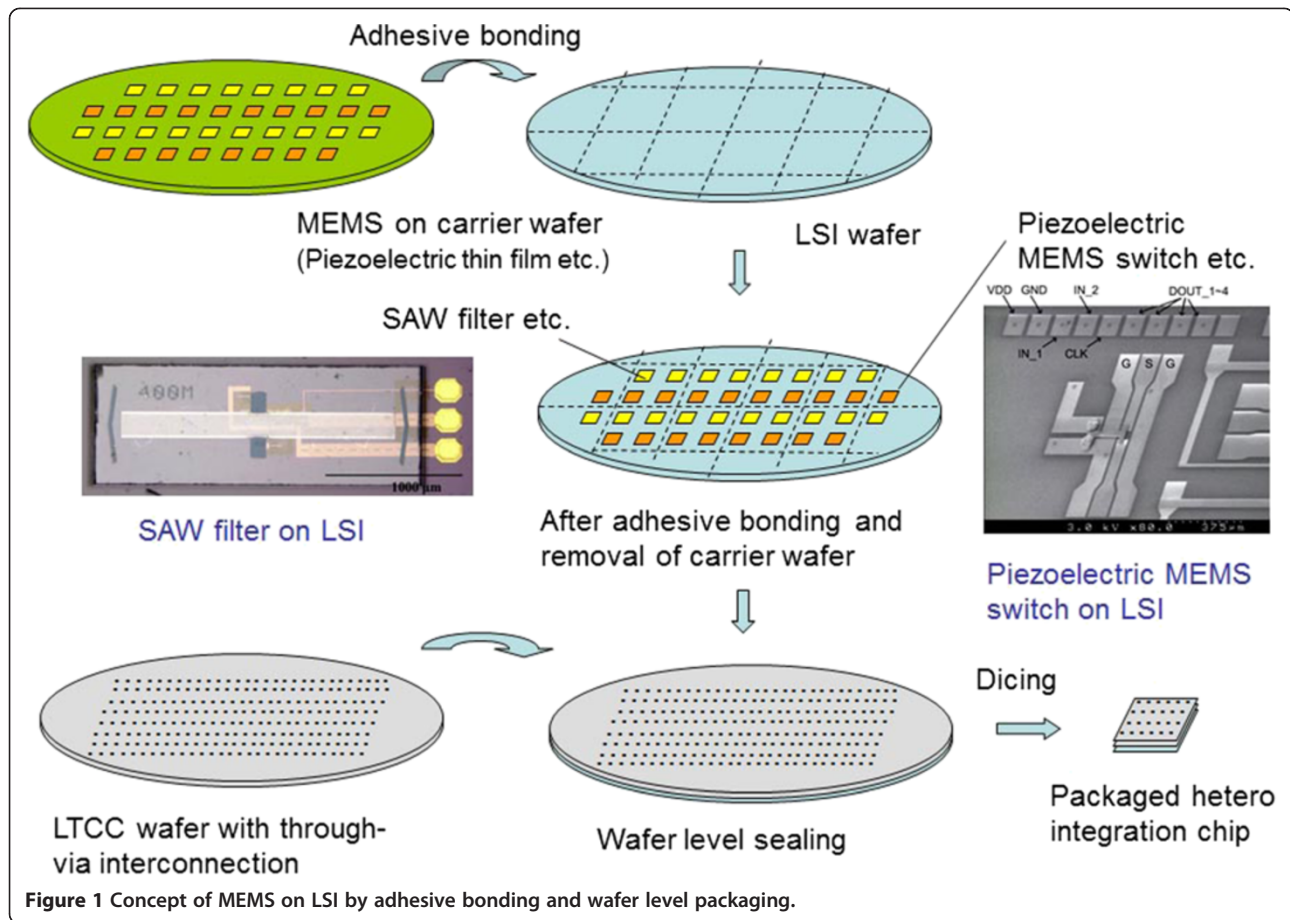
Various adhesive bonding methods have been developed [3]. The adhesive wafer bonding can be applied not only to the wafer level heterogeneous integration but also other purposes as three-dimensional IC, wafer-level packaging or microfluidics [4]. The wafer level transfer using the adhesive bonding has been studied in KTH in Sweden [5]. The heterogeneous integration processes are shown in Figure 3. These can be categorized to film transfer process (Figure 3(a) and II), (b) device transfer process (via-last) (Figure 3(b) and III) and (c) device transfer process (via-first) (Figure 3(c) and IV). The details and applications of these processes will be described below in II, III and IV. These heterogeneous integration processes can be applied not only to integrated MEMS but also to other devices as integrated optical devices by bonding a compound semiconductor wafer for laser or LED to a CMOS LSI wafer.

Film transfer process

The process can be used to transfer a film from the carrier wafer to the LSI wafer as shown in Figure 3 (a). After the adhesive bonding, the carrier wafer is removed and the remained film is used to fabricate MEMS devices on the LSI wafer. The MEMS fabrication process on the LSI wafer has to be compatible with the integrated circuit.

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A. Monocrystalline-Si mirror array on CMOS LSI

A high resolution SLM (spatial-light-modulator) chip with 1 million tilting micromirrors made of monocrystalline Si was developed [6]. The fabrication process and the photograph are shown in Figure 4. The mirror exhibits low surface roughness and drift free operation comparing metal mirror because of the creep-free mechanical properties of the monocrystalline Si.

B. CMOS-FBAR voltage controlled oscillator

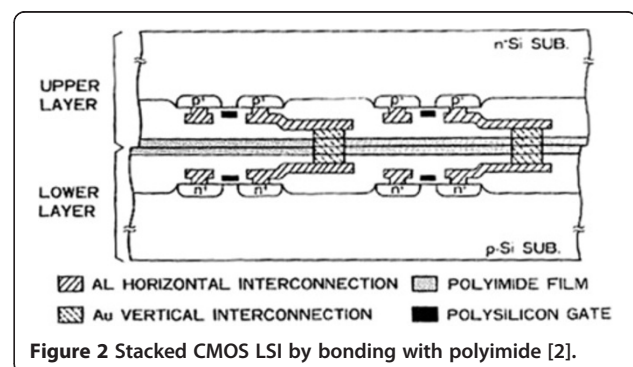
A wide-tuning CMOS-FBAR (film bulk acoustic resonator) based VCO (voltage controlled oscillator) for 2.45 GHz has been developed on 0.18 μm CMOS LSI [7]. The fabrication process, the circuit and the photograph are shown in Figure 5. Thin Si layer is formed on the CMOS wafer by adhesive bonding of a flipped SOI by BCB (benzocyclobutene) and removal of handle Si layer. A Ru and an AlN is sputter deposited and patterned respectively. Top Al electrode is fabricated by lift-off. Sacrificial etching is performed to remove the Si and the BCB underneath the FBAR to make an air gap. The circuit is a Pierce oscillator in which electrical frequency tuning can be done by connecting capacitors digitally.

Device transfer process (via last)

The device transfer processes have advantages that the MEMS can be fabricated independently from the LSI wafer. This enables wide range and optimized MEMS structures on LSI. In the via-last process the electrical interconnections from the MEMS to the LSI are made by metal vias after the transfer as shown in Figure 3 (b).

C. PZT MEMS switch

PZT (lead zirconate titanate) actuated MEMS switches were fabricated on a LSI wafer as shown in Figure 6 [8].



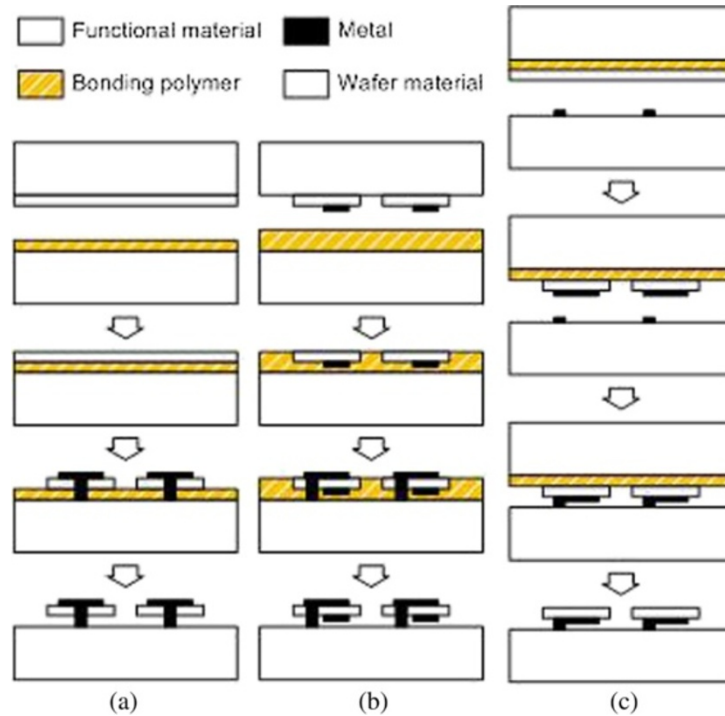


Figure 3 Heterogeneous integration processes; (a) Film transfer process, (b) Device transfer process (via-last), (c) Device transfer process (via-first).

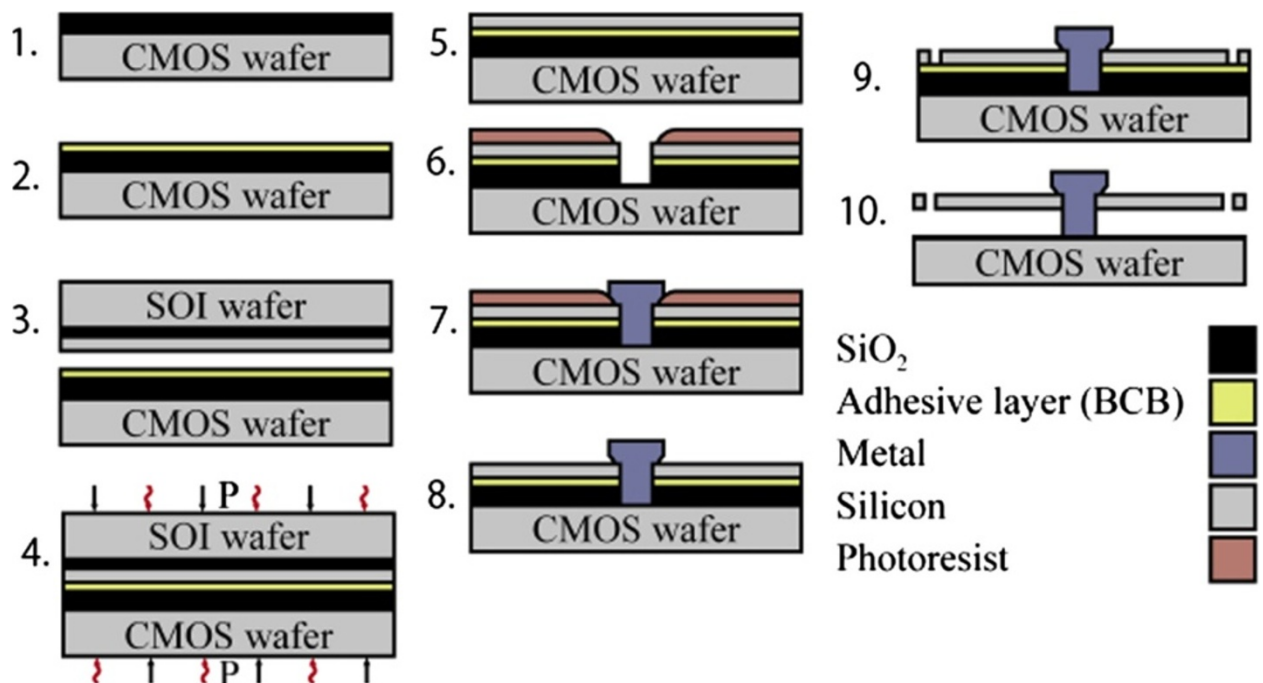


Figure 4 Monocrystalline-Si mirror array on CMOS wafer [6].

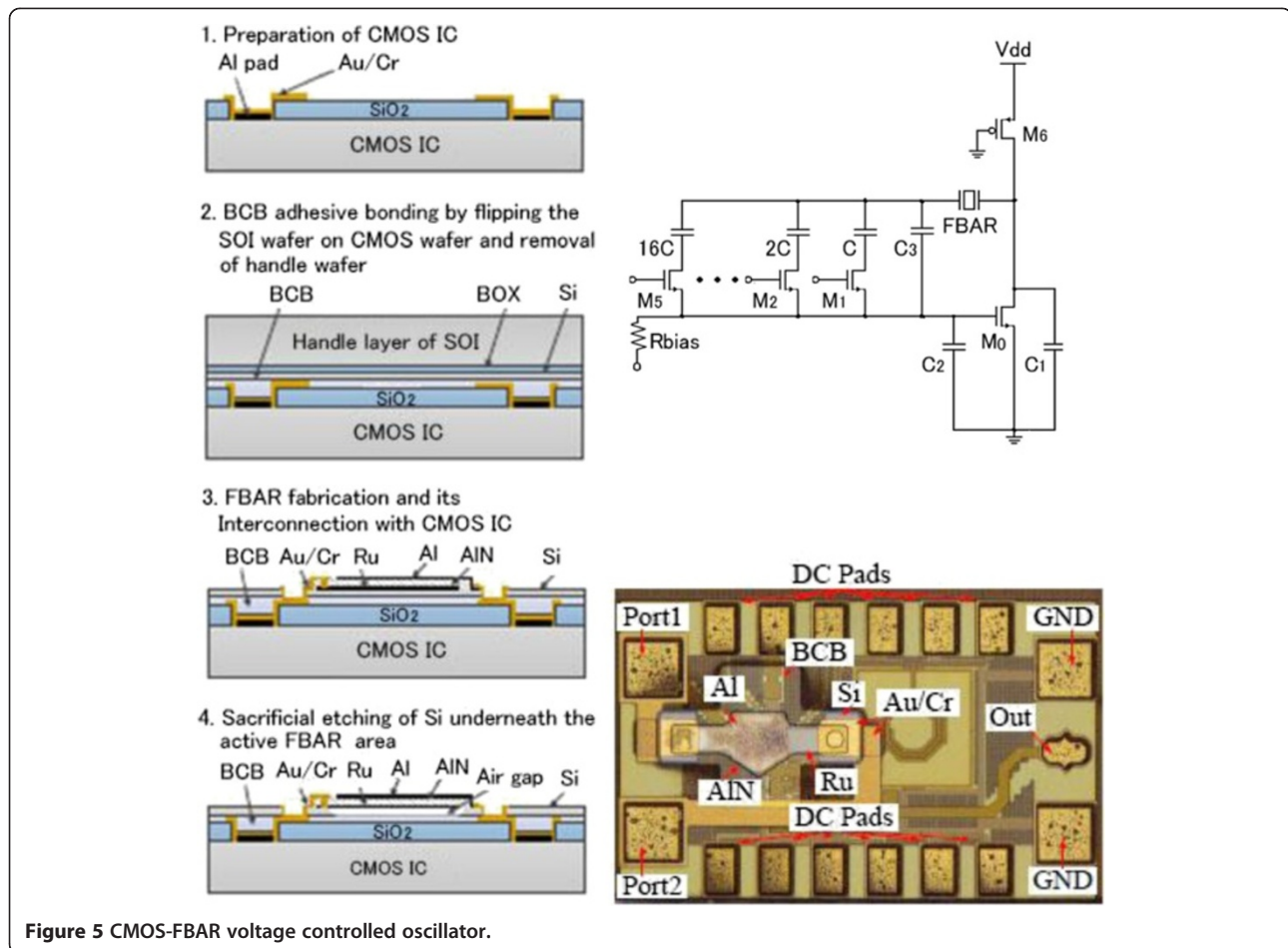


Figure 5 CMOS-FBAR voltage controlled oscillator.

The piezoelectric MEMS switch works at lower driving voltage and occupies smaller area than electrostatic MEMS switches. For the MEMS switch, the PZT was deposited on a Si wafer by a sol-gel method. In order to prevent a bending symmetrical structure made of two stacked PZT layers is formed and then patterned into device structures. They are transferred to the LSI wafer using the adhesive bonding. After connecting the MEMS and the LSI using electroplated vias, the polymer was removed by O₂ plasma to release the MEMS switches. The PZT cantilever bended downward by 6 μm by applying 10V to the lower PZT layer. The piezoelectric MEMS also enable wide range variable MEMS capacitors owing to their no pull-in phenomena comparing to the electrostatic MEMS.

D. Infrared Imager

Array of free-hanging poly Si bolometer was developed for CMOS-based uncooled infrared imager [9]. The fabrication process and the photograph are shown in

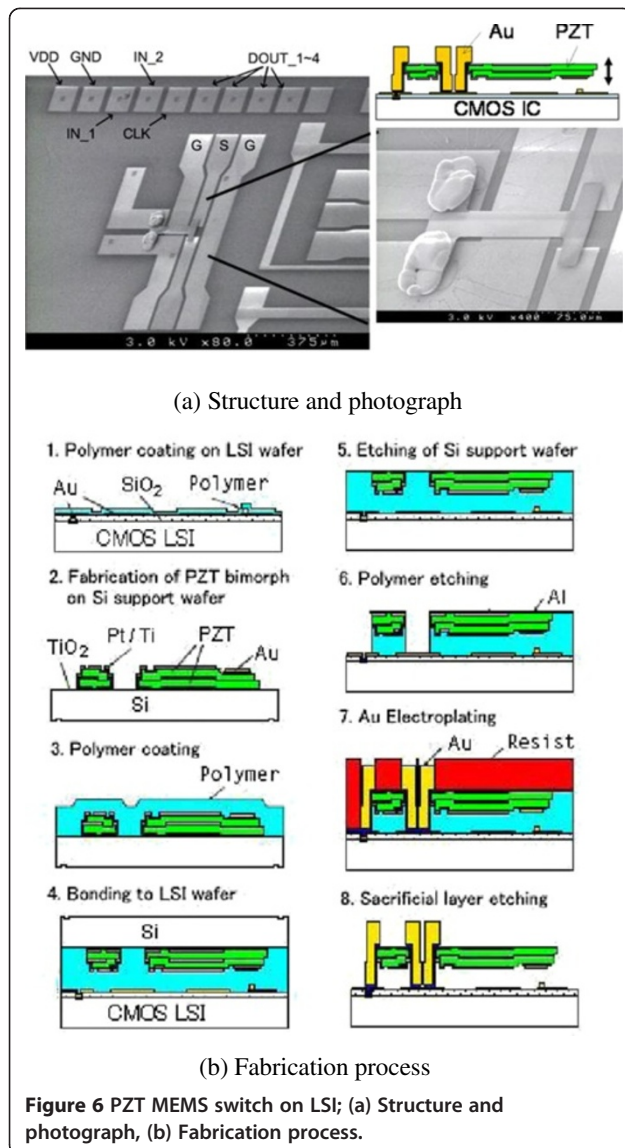
Figure 7. The via last device transfer was applied for this process.

E. Tactile sensor network

Distributed tactile sensors (tactile sensor network) are needed on the skin of robots to ensure their safety. These enable practically applicable nursing care robots and so on. A tactile sensor network which acquires sensing data from each tactile sensor element by autonomous data transmission (event driven) is shown in Figure 8 [10]. The tactile sensor chips are connected to a flexible cable having common 4 wires for power, ground and signal lines as shown in the photograph. Capacitive tactile force sensors were formed on a communication LSI by adhesive bonding using the BCB. The function of the communication LSI for the event driven data transmission was confirmed.

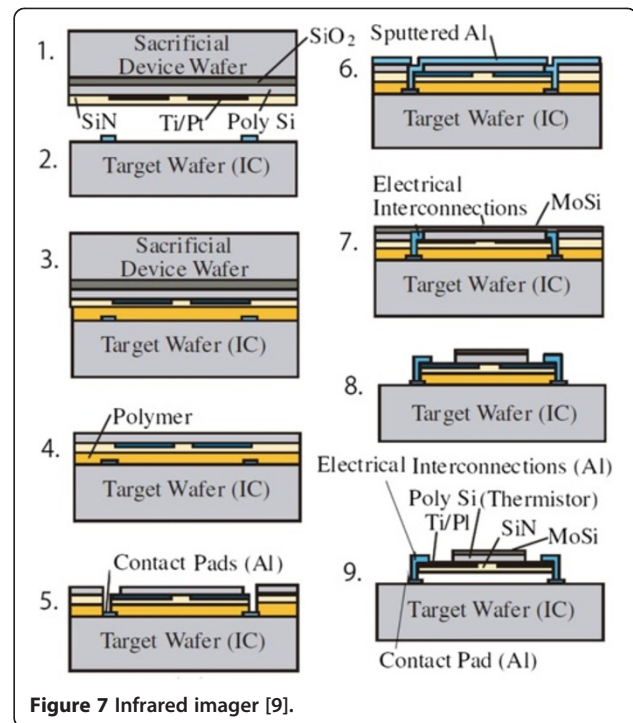
Device transfer process (via-FIRST)

The via-first device transfer process from the carrier wafer to the LSI wafer uses metal bumps for the



electrical interconnection and the mechanical holding of MEMS devices as shown in Figure 3(c). The metal to metal bump bonding methods as metal compression bonding and solder bonding can be used. There are some variations of the solder bonding as eutectic bonding or TLP (transient liquid phase) bonding which is called SLID (solid-liquid Inter-diffusion bonding) as well. The via-first process does not need electrical interconnection after the device transfer.

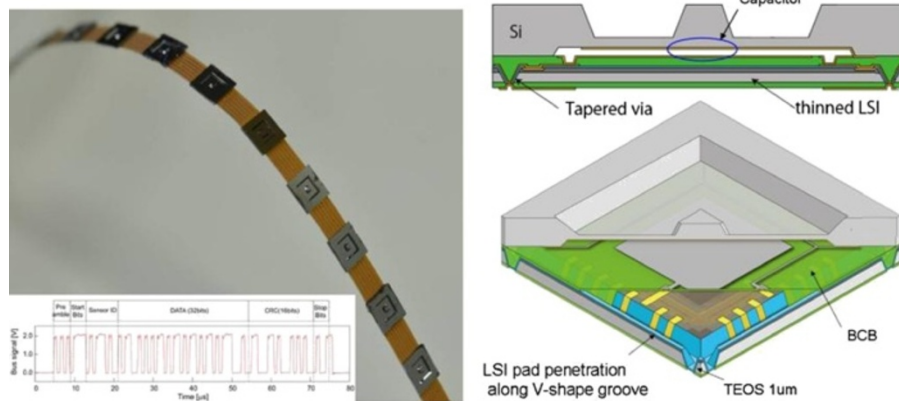
Adhesives are not mandatory for the via-first device transfer process but are used for temporary bonding of the devices on the carrier wafer or for an underfill (mechanical support). The via-first device transfer process without adhesive bonding has been applied for manufacturing of combined three-axis



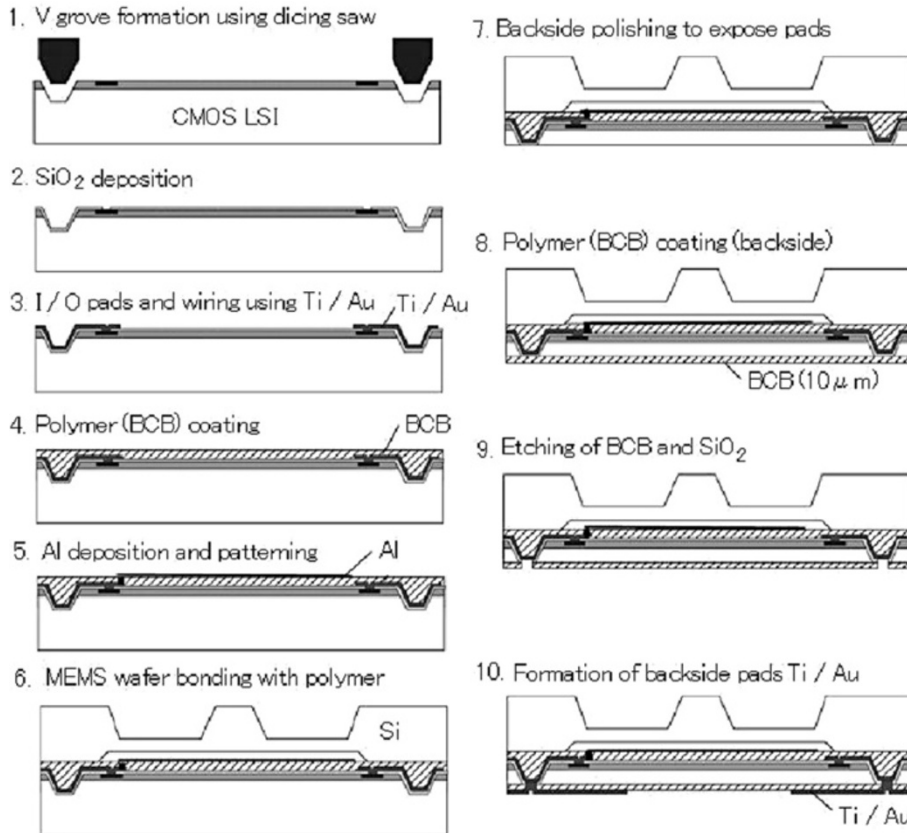
accelerometers and three-axis gyroscope at large volume for consumer product [11]. The MEMS wafer is used as a package and the process (Nasiri fabrication) uses Al/Ge eutectic bonding at 450°C for electrical interconnection and the package sealing simultaneously.

F. AFM based data storage (Millipede)

Fabrication process for arrays of AFM (atomic force microscope) probe on CMOS LSI is shown in Figure 9 [12]. This was developed for a multi probe data storage called Millipede. The AFM probes fabricated on a SOI wafer is transferred by polyimide bonding to a glass wafer which has PTFE (Teflon) film on it and removal of the handle Si layer. Thereafter Cu-Ni-Ti and adhesive polyimide are patterned on the backside (1. MEMS process in Figure 9). Sn-Cu bumps are formed on a CMOS wafer (2. CMOS bump process in Figure 9). The MEMS wafer is bonded to the CMOS wafer (3. wafer-level heterogeneous integration process in Figure 9). The Sn melt at the bonding temperature (380°C) and diffuse into the Cu. This makes intermetallic compound of which remelting temperature is higher than 500°C and hence the devices stand post transfer soldering. This metal bonding is called TLP or SLID. Debonding of the glass wafer is done by laser ablation through the glass wafer and finally the polyimide used for the device transfer is etched out using O₂ plasma.



(a) Sensors on a flexible circuit, signal waveform and structure



(b) Fabrication process

Figure 8 Tactile sensor network; (a) Sensors on a flexible circuit, signal waveform and structure, (b) Fabrication process.

G. Active matrix electron emitter for massive parallel electron beam exposure systems

A prototype electron emitter array integrated with an active-matrix driving LSI has been developed for high-

speed massively parallel direct write EB (electron beam) exposure system [13]. A nc-Si (nanocrystalline silicon) emitter used is shown in Figure 10 (a). The nc-Si emitter consists of cascaded tunnel junction

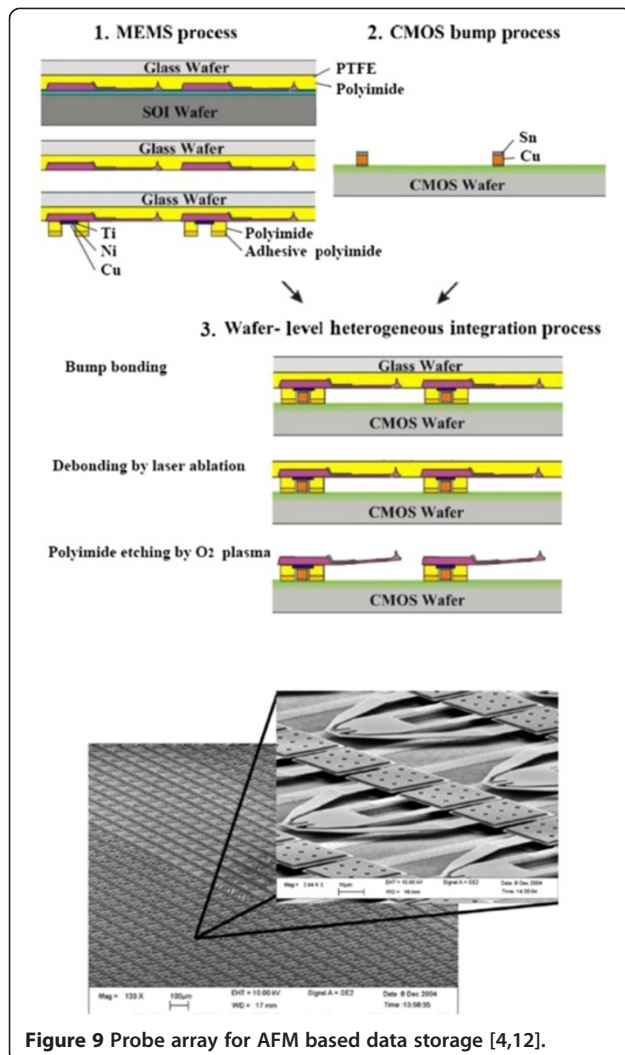


Figure 9 Probe array for AFM based data storage [4,12].

and hence the electron emission is controlled at low voltage (10V). A chromatic aberration is small because of a small energy dispersion of the emitted electron. The structure of the active matrix emitter is shown in Figure 10 (b) [14]. The nc-Si emitter is concave shaped in order to condense the electron and to collimate the electron beam using an extraction electrode, which is called Pierce gun. The wafer of the nc-Si emitter is bonded to a driver LSI wafer with gold bumps. 100×100 cells of the driver circuit are formed on a glass by adhesive bonding. The cells can be electrically isolated in order to apply a bias voltage to the cells for electronic aberration compensation. Photographs of the emitter-side and the bump-side of the nc-Si emitter wafer are shown in Figure 10 (c). Resist patterning by the emitted electron was successfully confirmed in preliminary experiment.

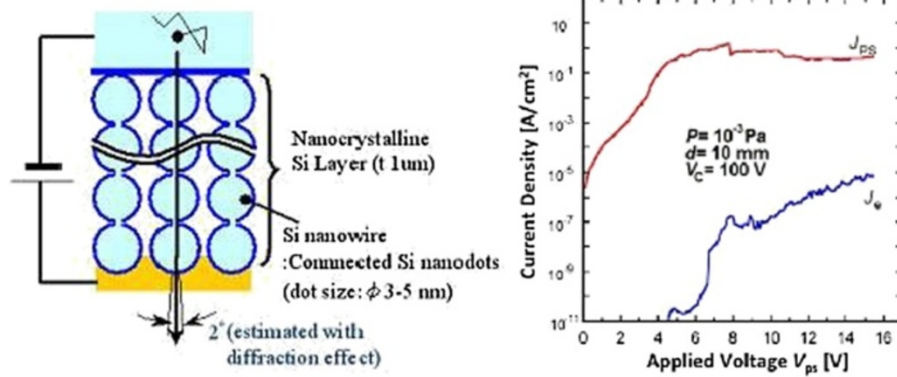
Selective transfer technologies

Wafer level selective transfer from one carrier wafer to multiple target wafers are needed for cost-effective integration of different chip sizes [15]. One example of the technology is shown in Figure 11 [16]. MEMS devices on a glass carrier wafer are bonded to the target LSI wafer (Figure 11 (2)) and MEMS devices to be transferred are debonded by laser through the glass carrier wafer (Figure 11 (3)). MEMS devices remained on the glass carrier wafer can be transferred to another target wafers (Figure 11 (4)).

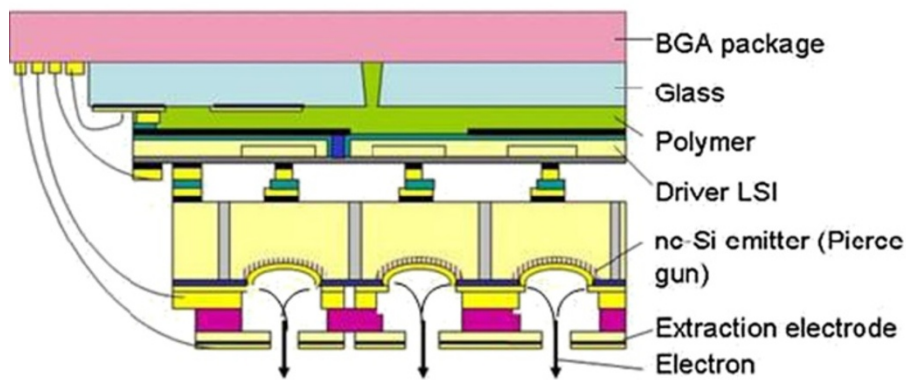
The selective transfer technology was applied to the SAW (surface acoustic wave) resonator on LSI as shown in Figure 12 [17]. SAW resonators are fabricated on a LiNbO₃ wafer and the wafer is bonded to a glass carrier wafer using an adhesive and diced to make grooves (1. LiNbO₃ SAW chip fabrication in Figure 12). The target LSI wafer is fabricated as follows. Metal (Au-Cr) pattern is made and sticky silicone bumps are also patterned on the wafer. Thereafter metal (Au-Cr) pattern is made on it (2. target silicon wafer fabrication in Figure 12). The flipped carrier wafer is bonded to the target wafer using the sticky silicone bumps. After debonding of the glass carrier wafer by laser the bump bonding is reinforced using an underfill polymer (3. integration/transfer in Figure 12). The photograph of the SAW resonators transferred on a LSI wafer is shown in Figure 12.

Conclusions

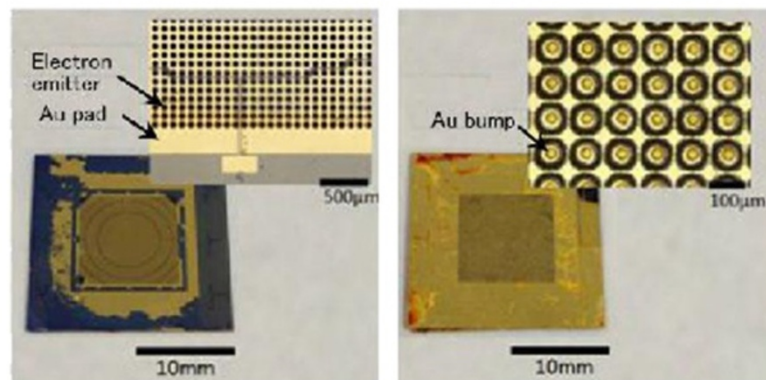
The heterogeneous integration on LSI using the wafer level transfer with adhesives is reviewed. This technology enables low cost production of value added devices. PZT which requires higher temperature than 600°C for depositing a thin film can be applied on LSI using this technology. Selective transfer from one wafer to multiple LSI wafers are described to cost effective production of different size MEMS chip from LSI chip. There are related items to this technology as adhesives, alignment for the bonding and debonding. The adhesives can be applied by coating, stamping and film laminating. The adhesive layers can be patterned or unpatterned and can stand relatively high temperature (400°C) as polyimide if needed. Transparent glass or self-alignment is required depending on the processes. There are various debonding methods to remove the carrier wafer as polymer etching, sacrificial layer etching and etching or mechanical grinding of the carrier wafer. In order to remove the polymer used for the wafer bonding polymer etching by ozone in acetic acid was developed [18].



(a) Principle and current of nc-Si emitter

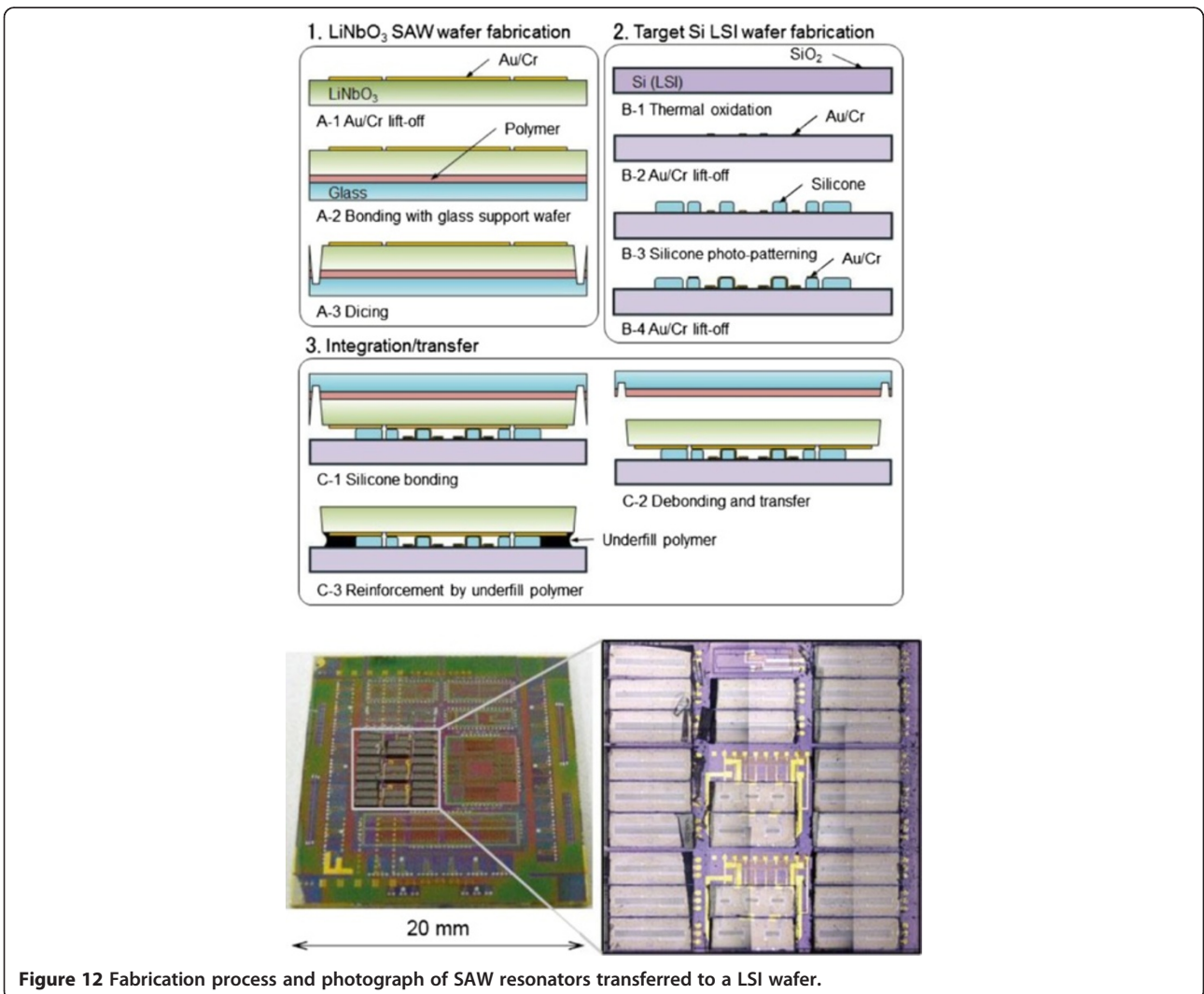
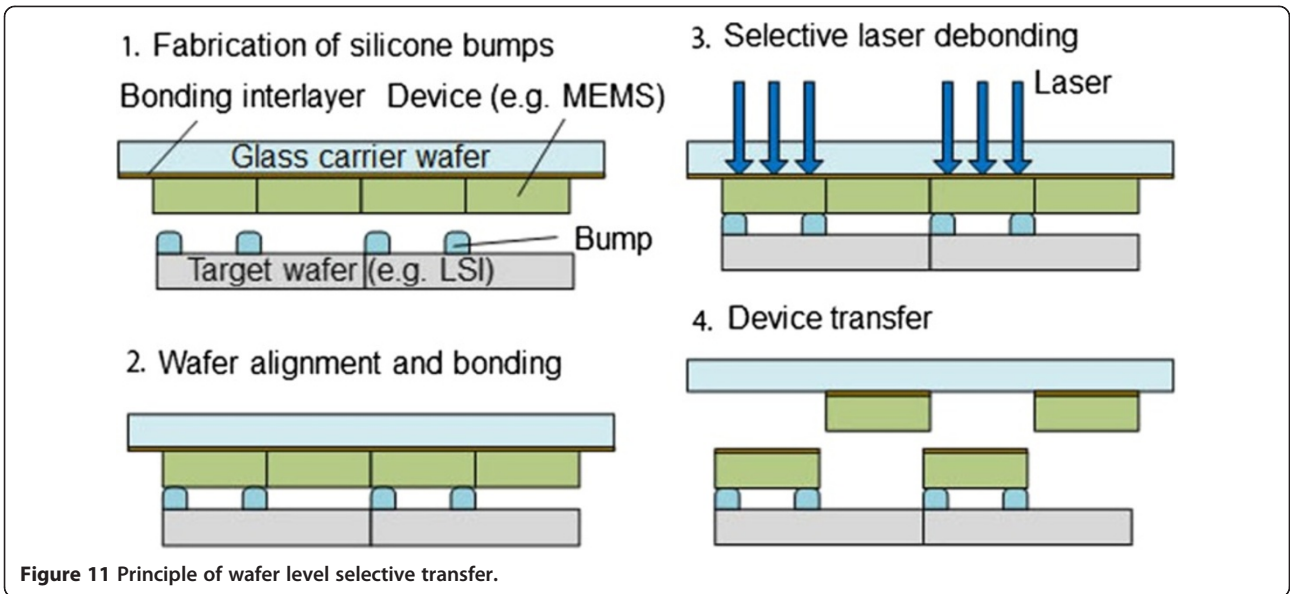


(b) Structure



(c) Photograph of the nc-Si emitter (Pierce gun) array

Figure 10 Active matrix nc-Si electron emitter; (a) Principle and current of nc-Si emitter, (b) Structure, (c) Photograph of the nc-Si emitter (Pierce gun) array.



Competing interests

The authors declare that they have no competing interests.

Authors' contributions

ME organized the research works and wrote the manuscript. ST carried out the development of the heterogeneous integration by adhesive bonding. Both authors read and approved the final manuscript.

Authors' information

Masayoshi Esashi received the B.E. degree in electronic engineering in 1971 and the Doctor of Engineering degree in 1976 at Tohoku University. He served as a research associate from 1976 and an associate professor from 1981 at the Department of Electronic Engineering, Tohoku University. Since 1990 he has been a professor and he is now in The World Premier International Research Center Advanced Institute for Materials Research (WPI-AIMR) and concurrently in Micro System Integration Center (μ SIC) (director) in Tohoku University. He has been studying microsensors, MEMS (Micro Electro Mechanical Systems) and integrated microsystems. Shuji Tanaka received B.E., M.E. and Dr.E. degrees all in mechanical engineering from The University of Tokyo in 1994, 1996 and 1999, respectively. From 1996 to 1999, he was Research Fellow of the Japan Society for the Promotion of Science. He was Research Associate at Department of Mechatronics and Precision Engineering, Tohoku University from 1999 to 2001, Assistant Professor from 2001 to 2003, and Associate Professor at Department of Nanomechanics from 2003 to 2013. He is currently Professor at Department of Bioengineering and Robotics. He was also Fellow of Center for Research and Development Strategy, Japan Science and Technology Agency from 2004 to 2006, and is currently Selected Fellow. He was awarded The Young Scientists' Prize, The Commendation for Science and Technology by the Minister of Education, Culture, Sports, Science and Technology in 2009 etc. His research interests include RF MEMS, MEMS-LSI integration and Power MEMS.

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