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Plasma dicing before grinding process for highly reliable singulation of low-profile and large die sizes in advanced packages

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Abstract

The demand for advanced packaging is driven by the need for low-profile, densely-integrated, large-die Si devices in substrate-based or wafer-level packaging. Die strength is a critical parameter for ultrathin dies, making die singulation a vital aspect of advanced packaging technology. In this work, we present a dicing before grinding (DBG) process to compare and analyze die strengths using a mechanical blade, stealth laser, and plasma dicing. The three DBG processes were applied to a 200 mm silicon (Si) wafer process with a die size of 10×10 mm^2 and thicknesses of 100, 200, and 300 µm, respectively. Optical and electron microscopes were employed to investigate chipping quality, sidewall damage, and surface contamination. The bare Si die's strength was assessed using a three-point bending test. Plasma dicing before grinding (PDBG) resulted in less contamination, chipping, and cracking compared to other DBG processes. Furthermore, PDBG exhibited the highest die strength of 1052 Pa.

Keywords Packaging, Plasma dicing, Blade dicing, Stealth dicing, Die strength

Introduction

Recently, technological challenges in the semiconductor industry have focused on extending Moore's law by developing ultrafine patterns of several nanometers to promote business growth. The limitations imposed by physical and electrical roadblocks on scaling have led to the development of 3D integration packaging using vertical interconnections by TSVs (through-silicon vias), such as high-bandwidth memory (HBM) and hybrid memory cubes (HMC). Generally, 3D integration technology includes 3D wafer-level packaging, 2.5D or 3D interposer-based integration, and 3D stacked IC integration, utilizing flip-chip technology to achieve vertical stacking and interconnection through redistribution layers (RDLs) and the bumping process. TSVs enable vertical interconnection from the front to the back side of IC chips for multiple device layers within a single chip area. Among the presented technologies, the trend is toward "More Moore," which involves the development of high-performance, highly integrated system chips in accordance with Moore's law [1]. State-of-the-art packaging technologies, such as embedded multi-die interconnect bridge (EMIB), Foveros, 3D fabric, and others, including TSV, enable the tight integration of discrete devices with distinct functions into minimal space. These advanced packaging technologies require low-profile, high-density integration while maintaining high reliability.

However, ultrathin wafers fabricated through mechanical thinning may be subject to residual stress. The dicing after grinding (DAG) process, which uses blade dicing, is widely employed for die singulation. Blade dicing is a mechanical cutting method that employs a blade saw to separate a wafer into individual dies simultaneously. This mechanical process can lead to microcracks on the die surface owing to the residual stress generated by wafer thinning. Improper die separation may result

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in cracks and brittleness, thereby reducing die strength [2–5]. Die strength becomes crucial as the wafer thickness decreases and die size increases, making the die more susceptible to cracking and breakage. Issues such as chipping, delamination, kerf geometry, die sidewall damage, and die surface contamination can arise due to insufficient die strength. High die strength is also necessary to withstand the mechanical and thermal stresses during post-processing and to ensure package reliability [6]. To improve the die strength using blade dicing process, dicing before grinding (DBG) has been introduced for ultrathin wafer singulation less than 50 μm. DBG is a singulation process that divides chips by first half-cutting the wafer using a dicing process, followed by backgrinding. For ultrathin die separation process technology, thinning, laser-based approaches, laser and mechanical hybrid methods, and plasma drawing are being developed to improve and enhance the quality [7]. Previous studies have investigated the effects of spindle and feed speeds on die strength under blade dicing conditions during the die separation process, as well as the correlation between chipping size and die strength after blade dicing.

In this study, we demonstrate and compare three types of DBG processes to propose a suitable singulation method for ultrathin wafer processing. We investigate the dependence of failure and fatigue strengths on the singulation method and thickness of Si dies using a three-point bending test. Furthermore, we determine the cause of the weakness in die strength to enhance the reliability of advanced packages.

Experimental procedure

Three types of DBG processes were employed to compare the die strengths of the bare Si dies [8–13]. We investigated die strength for three dicing processes: blade dicing before grinding (BDBG), stealth dicing before grinding (SDBG), and plasma dicing before grinding (PDBG). To compare and analyze die strength, we fabricated dies of the same size (10 mm × 10 mm) using a bare (100) Si wafer. For the BDBG process, half-cut blade dicing was performed at depths of 150, 250, and 350 μm on the wafer. A dicing saw (DAD3350; DISCO Co., Ltd.) was utilized for blade dicing. All other process conditions remained the same, except for the feed speed, which depended on the Si wafer thickness. The blade rotation speed was set at 30,000 rpm. The feed speed was 15 mm/s for half-cut depths of 100 and 200 μm, and 30 mm/s for the half-cut depth of 300 μm. Subsequently, we conducted backgrinding on each wafer to separate the dies. Finally, we performed the backgrinding and dry polishing until the remaining Si thickness reached 100, 200, and 300 μm, respectively.

In the SDBG process, a laser was focused at 50 μm from the surface of the wafer to form a belt-shaped modified layer (SD layer) within the Si wafer for thicknesses of 100 and 200 μm. For 300 μm thickness, a laser was additionally focused at 150 μm from the surface of the wafer to create two SD layers within the Si wafer. A fully automatic laser saw (DFL 7341; DISCO Co., Ltd.) was utilized for stealth dicing, and an SD layer was formed at a feed rate of 320 mm/s at 90 kHz. A standard beam of the laser saw was employed, and the laser output power was 0.9 W. Subsequently, we conducted backgrinding and dry polishing until the remaining Si thickness reached 100, 200, and 300 μm. The thinned Si wafer was attached to dicing tape and expanded to separate each die from the wafer during the SDBG process.

In the PDBG process [14], a photoresist was coated on a bare 8-inch Si wafer to a thickness of 15 μm. Photolithography was performed using a mask with a die size of 10 × 10 mm (Fig. 1a). After the photolithography process, a trench structure was fabricated using deep reactive-ion etching process, also known as the "Bosch process" (Fig. 1b). The etching equipment used was a GIGALANE MAXIS-NeoGENII, operated at atmospheric pressure and room temperature. The trench structure consists of one cycle of gas deposition and etching. The 280, 520, and 680 μm target depth substrates required 120, 220, and 320 cycles, respectively. A photoresist strip process was performed to remove the remaining photoresist under

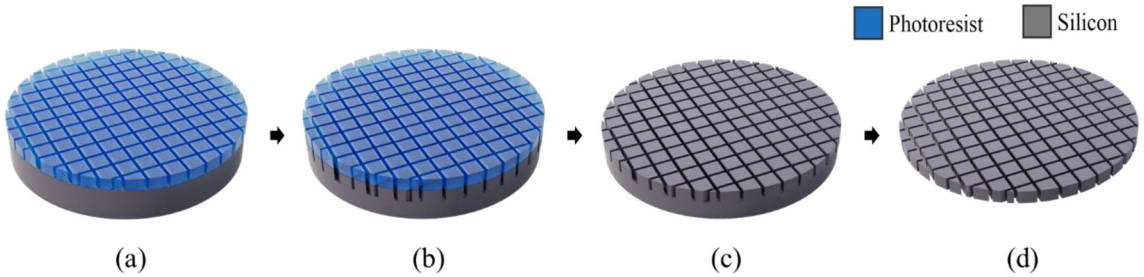

Fig. 1 Fabrication schematic of plasma dicing process: **a** photolithography of dicing lane, **b** Si deep reactive-ion etching process for Si trench, **c** ashing process to remove photoresist, and **d** grinding process of back side for die singulation

the conditions of 2500 W, 250 °C, for 120 s (Fig. 1c). We conducted a backgrinding process on each wafer to separate the dies in the same manner as in the BDBG process. The grinding process was performed for Si thicknesses of 100, 200, and 300 μm (Fig. 1d). A fully automatic grinder (DGP8760: DISCO Co., Ltd.) was used for grinding and dry polishing, which was commonly applied to the three previously described dicing methods. The process was performed in three stages: rough grinding in the Z1 spindle, fine grinding in the Z2 spindle, and dry polishing in the Z3 spindle. Depending on the thickness of the die to be manufactured, rough grinding was performed at 270, 370, and 470 μm in the Z1 spindle, and fine grinding was performed at a thickness of 45 μm in the Z2 spindle. Finally, in the Z3 spindle stage, dry polishing was conducted for 183 s at a force of 210 N. Thus, die separation was completed for the DBG process.

Results and discussion

After preparing the samples for evaluation, the appearance of the die was observed using optical microscopy and field-emission scanning electron microscopy (FE-SEM). The BDBG process successfully reduced the backside of the chip, as shown in Fig. 2b. The bottom of the sample was polished at the end of the grinding process and found to be smooth. However, a large amount of chipping was observed at the top edge of the die, due to the half-cut of the wafer by blade dicing, as shown in Fig. 2a.

In blade dicing, a wafer is mechanically cut using the frictional force between the blade and the Si. Chipping that occurs in the blade dicing process can be attributed to various factors, such as the diamond grit size attached to the blade, wafer orientation, dicing direction, cutting forces, coolant flow (deionized water), spindle speed, and feed speed [15, 16]. The size of the chips in the dies fabricated using blade dicing was approximately 10 μm. Debris was also observed on the top surface of the die due to the saw sludge or ground Si substrate, as shown in Fig. 2a. The sawing process used to separate the wafer into dies causes vertical edge cracks, which spread inward into the die because of tensile stresses [17].

In the SDBG process, chipping and contamination were not observed at the top edge of the die, as shown in Fig. 2a. While the SDBG process was a contamination-free dry process; however, internal voids, which were sharp cracks extending from the top surface to the bottom side, were observed on the SD layer in the sidewall of the die, as shown in Fig. 3a. Figure 3a presents the SEM image of the sidewall of the SDBG process. Several microcracks are observed along the voids. Microcracks and voids occur at the focal spot of the SD layer due to phase transformation from highly constrained melting and vaporization to cooling, as shown in Fig. 3a [18–20]. Voids in the SD layer-initiated cracks during the tape expansion process by applying tensile stress to the wafer. The width and pitch of voids were approximately 1 and 3 μm, respectively, which correspond to the feeding speed and repetition rate of 320 mm/s and 90 kHz.

The PDBG is a damage-free process. As shown in Fig. 2c, chipping and contamination in the top and bottom surfaces of the die or internal voids in the sidewall were not observed compared with the BDBG and SDBG processes. In the PDBG process, scallops were observed due to the Si trench etching using the Bosch process, as shown in Fig. 3b. The Bosch process used in plasma dicing is a high-aspect-ratio etching technique that repeatedly involves isotropic etching and passivation. A cycle of SF_6 plasma etched the exposed Si surface and a cycle of C_4F_8 plasma formed a passivation layer. This sequential process was repeated until the designated depth of the substrate was reached, resulting in a scallop on the

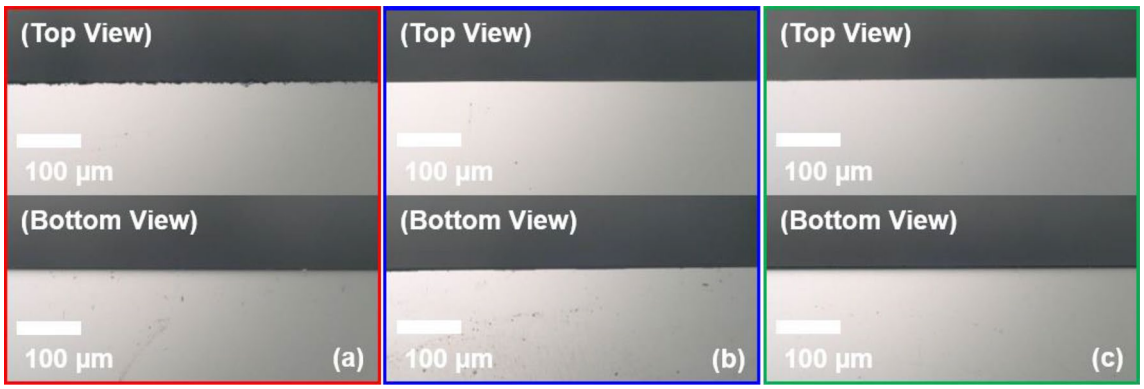

Fig. 2 Optical microscope image of Si dummy die using blade dicing, stealth dicing, and plasma dicing processes: **a** Die's top edge, **b** Die's bottom edge, **c** Die's side wall

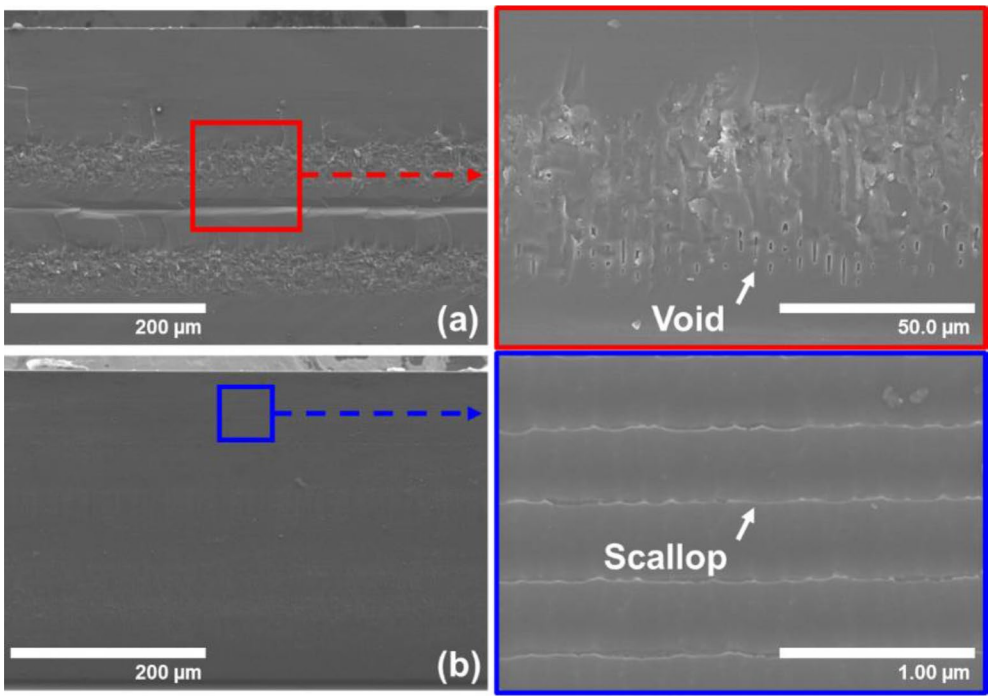

Fig. 3 Cross-sectional FE-SEM view of dies manufactured by **a** stealth dicing and **b** plasma dicing

sidewall. The scallop size during PDBG was approximately 400 nm.

The roughness of the diced surfaces was evaluated using Bruker Nano Surfaces and Metrology Division equipment. Figure 4 displays the surface roughness obtained by optically profiling the surface area of a diced surface with a measurement field of 400 μm × 300 μm. The surface roughness of the BDBG-processed diced surface appears very large, exceeding 500 nm from the top edge to a depth of about 50 μm, for the same reason as the chipping confirmed in Fig. 2a. The sidewall roughness beyond a depth of 50 μm can be considered excellent due to the polishing mechanism. The surface processed with SDBG exhibit a large roughness of 2000 nm at 150 and 50 μm near the SD layer, corresponding to the depth of laser irradiation. As confirmed in the SEM image (Fig. 3a), voids within the dicing surface and very high roughness, that attributed to the expansion process for die separation, were observed. The surface processed with PDBG exhibited an even overall roughness, and no sharp roughness due to scallops was observed. The parameters analyzed for surface roughness included Sku, an index representing the degree of sharpness, and the Sz value, which indicates the distribution of roughness. Sku represents kurtosis, which is a measure of the sharpness of the surface or the distribution of spikes above and below the mean line. Sz can be obtained as a ten-point average of the absolute heights of the five highest peaks and the deepest valleys. The Sku indices were 20, 18, and 3, and Sz was 1728, 9461, and 10,743 nm for PDBG, SDBG, and PDBG, respectively. While PDBG exhibits a very uniform distribution of roughness, including not only a specific region with a very large roughness but also a smaller distribution of roughness compared to other processes. As shown in Fig. 2a, a specific area with very large roughness corresponds to the chipping part, while the remaining areas display relatively even roughness. Based on these results, it can be assumed that the fact that BDBG and SDBG, compared to PDBG, the low die strength observed, are significantly correlated. This implies that PDBG, which exhibit a relatively wide and uniform roughness distribution compared to the other processes, is associated with the highest die strength.

To effectively compare the reliability of the fabricated dummy chips, we measured the die strength using a three-point bending test, G86-0303, following the Semiconductor Equipment and Materials International (SEMI) standard [21–27]. The three-point bending test is commonly employed to examine the effects of shape, surface treatment, and die geometry on die strength for large and deep cracks generated during the wafer-thinning process based on linear beam theory [3, 12]. The dummy chip was positioned on two supporting pins located at 1/3 point from both sides of the die (Fig. 5). The top side of the dummy chip was moved upward to induce a vertical die crack, which is one of the major failure models in

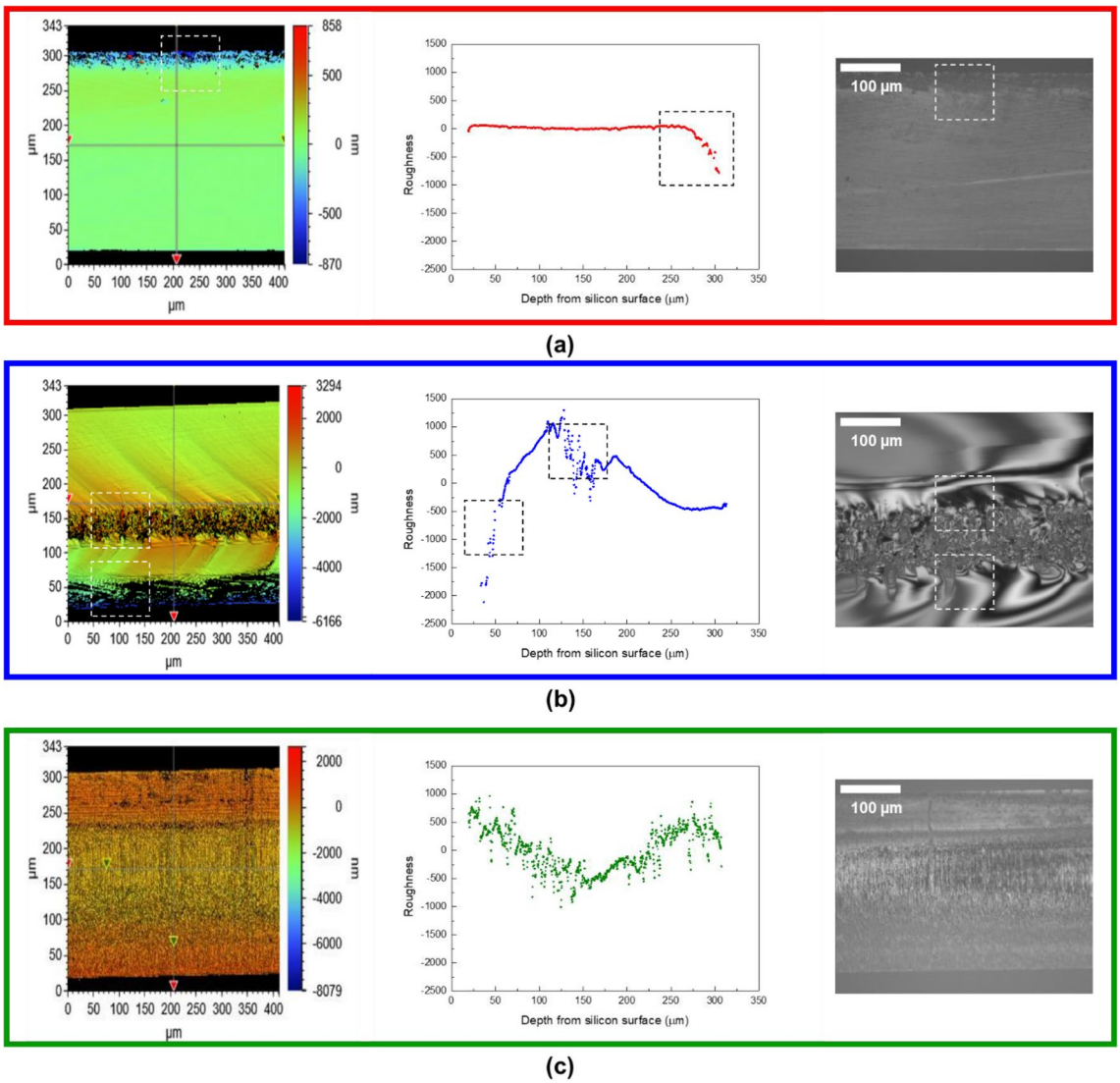

Fig. 4 A visualized contour map, its contour graphs and SEM images to analyze the surface roughness of the diced surface using **a** BDBG, **b** SDBG, and **c** PDBG

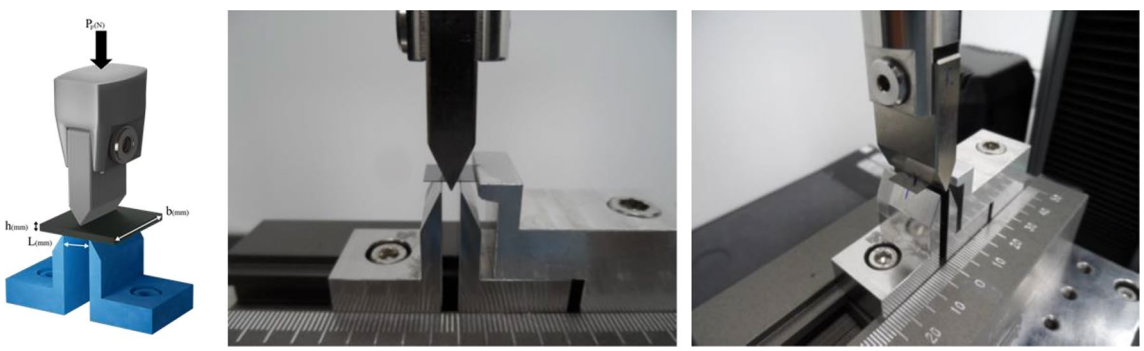

Fig. 5 Schematic and pictures of die strength measurement by 3-point bending

a flip-chip package under thermal loads. Vertical cracks initiated from surface defects of the die and propagate inward into the chip simultaneously as stress is applied, resulting in failure. Die strength was measured and calculated by applying a force using a loading pin at the center of the dummy chip. The loading pin continuously increased displacement at a speed of 0.5 mm/min, raising the force until the die broke. The die strength was derived from the beam theory using the formula: $\sigma_p = 3P_pL/2bh^2$, where P_p represents the loading force on the specimen; L is the distance between the two supporting pins (300 μm); b and h are the width (10 mm) and thickness (100, 200, and 300 μm) of the specimen, respectively.

The experiment involved randomly selecting 15 samples per wafer under each condition. The experimental result from the 3-point bending test for Si dummy die with a thickness of 100 μm showed die strengths of 1023, 333, and 1584 MPa for BDBG, SDBG, and PDBG, respectively, as shown in Fig. 6a. Moreover, for dummy die with a thickness of 200 μm, increased die strength of 724, 293, and 1344 MPa were observed for BDBG, SDBG, and PDBG, respectively, as shown in Fig. 6b. Similarly, at a thickness of 300 μm, the die strengths were 502, 354, and 1052 MPa, as shown in Fig. 6c.

The experimental results demonstrated a relatively higher die strength compared to those found in previous studies. In a previous study, die strength was assessed using a sample that still had wheel marks from the grinding process. In contrast, this study involved a dry polishing process immediately following the thinning process, effectively removing wheel marks. As a result, chipping on the bottom surface of the dummy Si chip, which can lead to artificial cracks, was reduced. The surface treatment applied to the dummy chip also contributed to a significant increase in die strength. However, the SDBG process led to lower die strength owing to the presence of microcracks on the sidewall. Microcracks, originating from the SD layer, serve as an artificial crack and cause failure crack to propagate along the longitudinal or transverse direction of the (100) plane of the Si dummy chips. The PDBG process demonstrated greater die strength compared to the other methods, as shown in Fig. 6, because there were no cracks such as chipping or internal voids. Specifically, the scallop structure on the sidewall of the dummy die did not act as an artificial crack and had no impact on die strength. To summarize the experimental results, Table 1 lists the average maximum forces, deflections, and corresponding die strengths for the fabricated dummy die.

Conclusions

In conclusion, this study introduced a highly reliable die signaling process for thin wafers using PDBG, which was compared to BDBG and SDBG methods. The dry polishing of the BDBG process enhanced die strength compared to the typical DAG process, but surface debris on Si die resulted from sludge or ground Si substrates. Both SDBG and PDBG exhibited contamination-free singulation, making them ideal for photonic and optical devices. However, microcracks were observed on the SD layer in the Si die sidewall using the SDBG process, resulting in low fracture resistance. The PDBG process also provided a damage-free signaling process, as confirmed by the three-point bending test. With the growing demand for low-profile and large die sizes, die singulation using the PDBG process is promising for an advanced packaging technology with high reliability.

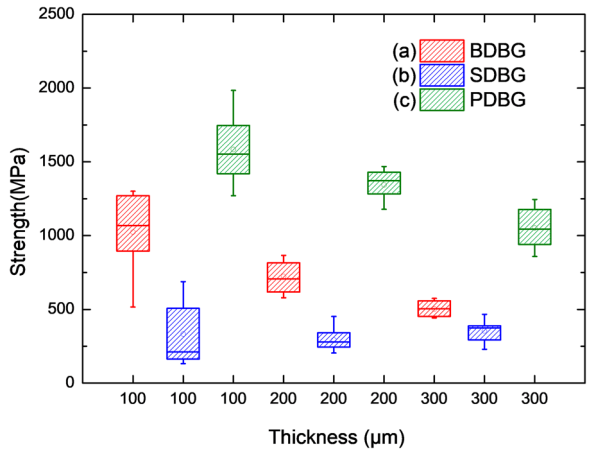

Fig. 6 Die strength of Si dummy die using **a** BDBG, **b** SDBG, **c** PDBG processes by 3-point bending test

Table 1 The results of average maximum forces, deflections, and corresponding die strengths for the fabricated dummy die

Test dies	Avg. P_{max} (N)	Avg. δ_{max} (mm)	Avg. σ (MPa)	S_d (MPa)
BDBG (μm)				
100	22.74	0.21	1023.41	274.08
200	64.31	0.11	723.53	96.37
300	100.48	0.07	502.41	50.18
SDBG (μm)				
100	7.40	0.07	333.10	191.35
200	26.3	0.07	292.82	69.46
300	60.98	0.06	304.91	104.23
PDBG (μm)				
100	35.20	0.29	1584.07	214.49
200	119.49	0.18	1344.32	94.47
300	210.47	0.17	1052.36	128.79

Abbreviations

BDBG	Blade dicing before grinding
DAG	Dicing after grinding
DBG	Dicing before grinding
EMIB	Embedded multi-die interconnect bridge
HBM	High-bandwidth memory
HMC	Hybrid memory cubes
MOTIE	Ministry of Trade, Industry & Energy
PDBG	Plasma dicing before grinding
SBID	Semiconductor Business Innovation Development
SDBG	Stealth dicing before grinding
SEMI	Semiconductor Equipment and Materials International
TSV	Through-silicon vias
RDL	Redistribution layers

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Author contributions
Conceptualization: KK, YN, and JP; methodology: KK, YN, KK (Kyoungmin Kim), TK, SK, and JP; validation: KK, YN, KK (Kyoungmin Kim), TK, SK, and JP; formal analysis: KK, YN, and JP; investigation: KK, YN, and JP; resources: KK, YN, and JP; data curation: KK and YN; writing—original draft preparation: KK and YN; writing—review and editing: KK and YN; supervision: JP; project administration: JP. KK and YN contributed equally to this work. All authors have read and agreed to the published version of the manuscript.

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Availability of data and materials
The datasets used and/or analyzed in the current study are available from the corresponding author upon reasonable request.

Declarations

Competing interests
The authors declare that they have no competing interests.

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